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FIFOs Using Virtex-II Shift Registers

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Summary

The shift registers available in Virtex™-II devices are ideal when building synchronous FIFOs. By using the flexibility of the shift register LUT primitive (SRL16), FIFOs can be built with any width while producing a 1-bit resolution. With cascaded SRL16 shift registers (SRLC16), a flexible depth in multiples of 16 is available.

Introduction

This application note describes a synchronous FIFO built using the SRL16 shift registers. This includes synthesizable code for configuring FIFOs of any width and depths of 128, 512, 1K, 2K and 4K bits.

The SRL16 shift registers are ideal for building smaller synchronous FIFOs. These shiftregisters are actually configured using the Look Up Table (LUT) and do not use flip-flops available in the slice. Hence they become useful in a design with little logic left to build the FIFO. When building bigger FIFOs the available block RAM in Virtex-II devices should be used.

FIFOs Using the SRLC16 Shift Registers

Figure 1 is a block diagram of a synchronous FIFO. A binary up/down counter is used to generate the READ and WRITE addresses. Table 1 lists the port definitions for a synchronous FIFO design. The address is incremented for a write and is decremented for a read. The design is also used for simultaneous read and writes.

Table 1: **Port Definitions**

Signal Name	Port Direction	Port Width
CLK	Input	1
SINIT	Input	1
WR_EN	Input	1
RD_EN	Input	1
DATA_IN[N:0]	Input	N+1
DATA_OUT	Output	N+1
FULL	Output	1
EMPTY	Output	1
DATA_COUNT[C:0]	Output	C+1

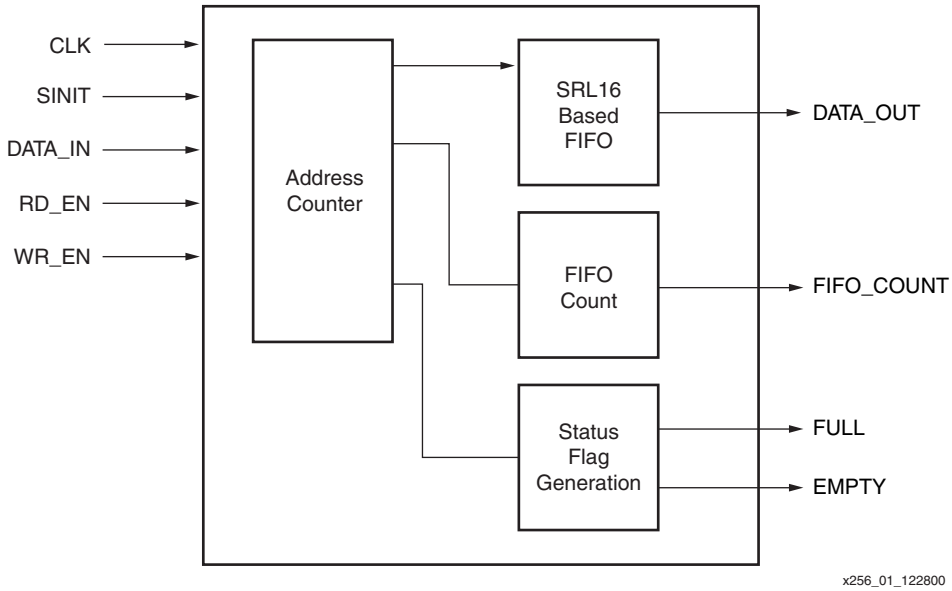

Figure 1: **Synchronous FIFO Using SRLC16 Shift Registers**

Synchronous FIFO Operation

To perform a write, the write enable signal is driven high prior to a rising clock. Before performing a write check the FIFO to make sure it is not FULL. The address for the write is provided by the address counter.

To perform a read, the clocking of data into the FIFO is disabled. For future writes the address from the address counter is decremented by one. The registered data to be read is available on the output of the MUX in the SRL16 register. It is available on the data output port. To show how full the FIFO is, the address counter is also used as a data counter.

The FULL flag is generated when the FIFO is full and no more data can be written into the FIFO. For a 128-bit deep FIFO, the FULL flag is generated when data is written into the 128th address location. The EMPTY flag is generated when the FIFO is empty and no more data can be read from the FIFO.

Design Resources

By using one CLB and cascading eight SRLC16 shift registers, a128-bit deep FIFO is generated (Figure 2). Using the multiplexers F5, F6, and F7, multiplexes the output of the four shift registers. Similarly a 256-bit deep FIFO is generated using two CLBs and one more multiplexer, (F8). Generate synchronous FIFOs of any width by instantiating as many cascaded shift registers as required.

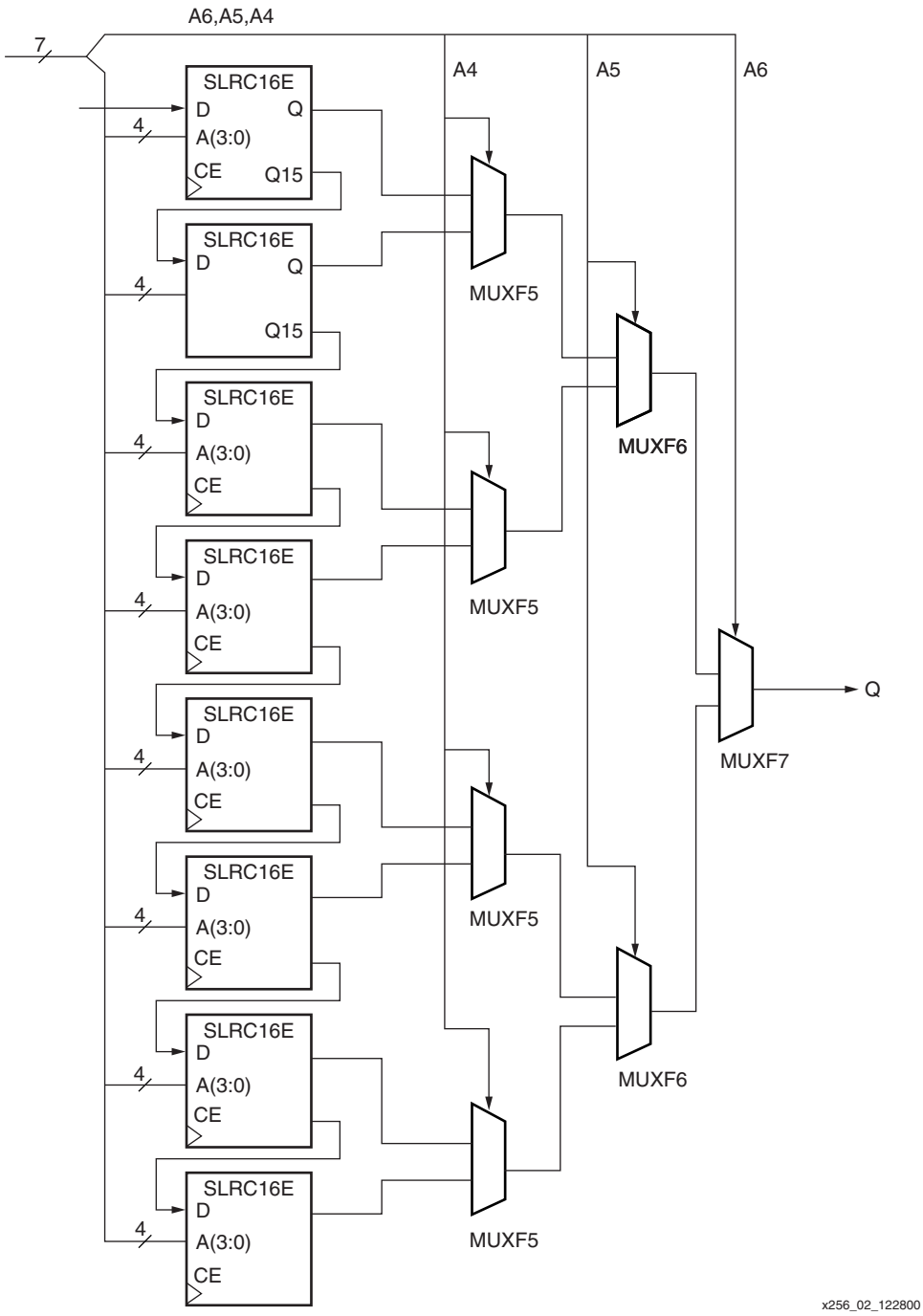

Figure 2: **Generating a 128-Bit Deep FIFO Using SRLC16E Modules**

Reference Designs

The application note provides designs with 128-bit, 512-bit, 1K, 2K and 4K bit deep FIFOs of any width. The reference design is available in both VHDL and Verilog files.

Design	Description
FIFO128.vhd, .v	128-bit deep synchronous FIFO
FIFO256.vhd, .v	256-bit deep synchronous FIFO
FIFO512.vhd, .v	512-bit deep synchronous FIFO
FIFO1k.vhd, .v	1Kb deep synchronous FIFO
FIFO2k.vhd, .v	2Kb deep synchronous FIFO
FIFO4k.vhd, .v	4Kb deep synchronous FIFO

Conclusion

Building synchronous FIFOs using the SRLC16 shift registers is an ideal solution for data storage when block RAMs are unavailable.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/15/01	1.0	Initial Xilinx release.